



## SmartWORKS Recording Performance

Revision	Date	Notes	Initials
0	8/12/2005	Initial draft	JAB/GMS

### ***Purpose***

The purpose of this document is to report the results of performance testing conducted on Ai-Logix SmartWORKS products within the context of channel density.

### ***Background***

The SmartWORKS SDK is designed to allow a maximum of 512 channels and 32 boards per chassis. In practice, the actual number of channels that can be run simultaneously will vary depending on many external factors such as the Codec compression rate, the CPU speed, and application architecture. Because of the PCI bus interface bandwidth bottle necks, using  $\mu$ -law or A-law CODECs, with a bandwidth of 64 kbps (kilo-bits per second) allow for fewer channels while using a G.723.1 CODEC running at 5.3 kbps allows for more.

It is important to consider the architecture of Windows operating systems and it's interaction with the Ai-Logix SDK. The SmartWORKS SDK and boards are memory mapped into the systems memory space via the PCI bus. Anytime data is read from or written to the boards, the system CPU is held off in suspension until the cycle is completed.

Once the total time for PCI accesses is taken from the available CPU cycles, what remains must be sufficient for the host based processing of SmartWORKS.

### ***Test Methodology***

The results of this test were measured using a program called SmartBENCH Version 1.0.0.0. This is a program written by Ai-Logix that simulates a simple recording application while also measuring CPU utilization. This program can be downloaded from the Ai-Logix support site.

CPU utilization was calculated by measuring how long it took to perform a fixed task. By using a lower priority thread running a dummy process, the program can keep track of how many cycles it has used. This thread is run after startup, prior to starting SmartWORKS, to estimate the baseline amount of CPU available with just the Windows overhead presently running.

The test application, for each tested audio CODEC, proceeds to start five channels streaming recorded data, which is written to five files, one for each channel. After each channel reports that streaming started, the CPU utilization



thread is reset to zero cycles and is allowed to run through several iterations. The CPU utilization thread is then commanded to stop and report the number of iterations it performed versus the number of system ticks. This number is compared against the baseline computed earlier to determine CPU utilization.

The test application then proceeds to add an additional five channels and repeat until 95% estimated utilization occurs or all available channels are streaming.

## **Test Systems**

Two basic systems were tested: a single CPU Pentium 4 and a Dual Xeon computer. All configurations tested used Windows 2000 SP4 5.00.2195 and Ai-Logix SmartWORKS SDK 3.5.1 Build 492.

### **Configuration 1**

- Pentium 4 2.66GHz Northwood 533 FSB
- Intel i845G Motherboard (Limit of 14 PCI slots)
- 256MB PC3200 DDR SDRAM
- Western Digital Caviar 80GB 7200RPM ATA100 8MB Cache

### **Configuration 2**

- (1) Intel Xeon 2.8GHz Prestonia 533MHz FSB
- Intel SE7501HG2 Motherboard (Limit of 6 PCI slots)
- (2) 512MB PC2100 DDR SDRAM Registered ECC
- Western Digital Caviar 80GB 7200RPM ATA100 8MB Cache
- Hyperthreading disabled

### **Configuration 3**

- (1) Intel Xeon 2.8GHz Prestonia 533MHz FSB
- Intel SE7501HG2 Motherboard (Limit of 6 PCI slots)
- (2) 512MB PC2100 DDR SDRAM Registered ECC
- Western Digital Caviar 80GB 7200RPM ATA100 8MB Cache
- Hyperthreading enabled

### **Configuration 4**

- (2) Intel Xeon 2.8GHz Prestonia 533MHz FSB
- Intel SE7501HG2 Motherboard (Limit of 6 PCI slots)
- (2) 512MB PC2100 DDR SDRAM Registered ECC
- Western Digital Caviar 80GB 7200RPM ATA100 8MB Cache
- Hyperthreading enabled

## Conclusions

The results of these tests show a strong link between the CODEC and the number of channels. As the amount of data that has to transverse the PCI interface increases, the number of channels for a given CPU utilization level decreases.

The following conclusions are important to note:

1. If the CODEC bit rate is kept to 16Kbps or lower, most standard PCs are capable of supporting up to 450 channels at less than 80% CPU utilization.
2. On average, a system with Hyperthreading enabled will give a 30% increase in channel count.
3. On average, the DP performs approximately 10% better then the NGX.

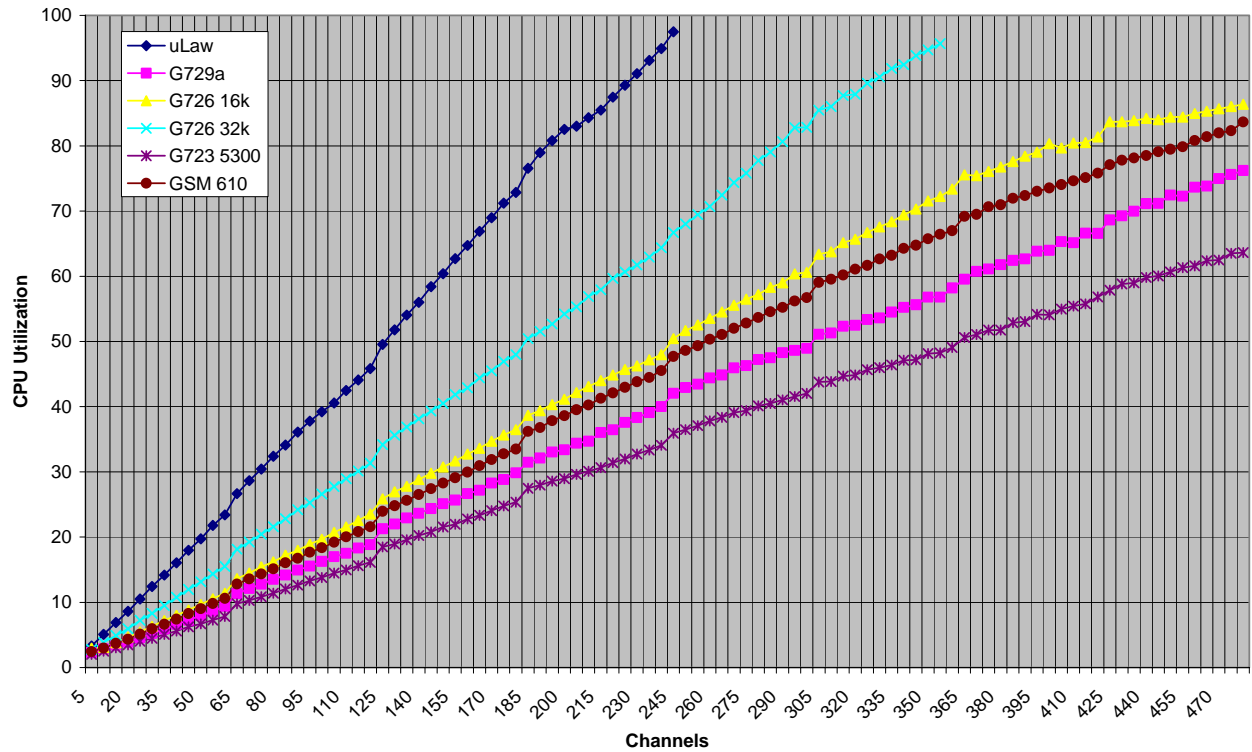
Table 1 represents a summary of the measured results. The data shown is the number of channels measured at a 50% CPU utilization for each configuration and each CODEC. The 50 percent mark was chosen no other reason other than it is a midpoint and allows a generous margin for actual user applications.

Test Configuration	CODEC	Board Type	# of Channels	% Utilization	Board Type	# of Channels	% Utilization
Configuration 1 Pentium 4 2.66GHz	μ-Law	DP	125	49.57%	NGX	105	49.84%
	G726 32k		185	50.43%		165	49.45%
	G726 16k		245	50.43%		220	50.70%
	GSM		260	50.53%		260	49.77%
	G729a		305	51.09%		270	50.12%
	G723		365	50.63%		345	50.01%
Configuration 2 Single Xeon No Hyperthreading	μ-Law	DP	130	50%	LD	140	50.16%
	G726 32k		210	49.96%		225	50.85%
	G726 16k		290	50.12%		300	50.15%
	GSM		325	50.23%		330	50.52%
	G729a		370	50.13%		375	50.40%
	G723		440	50.11%		450	50.15%
Configuration 3 Single Xeon With Hyperthreading	μ-Law	DP	170	50.51%	LD	180	49.39%
	G726 32k		295	50.47%		275	49.81%
	G726 16k		360	50.23%		350	49.86%
	GSM		415	49.95%		415	50.19%
	G729a		475	50.32%		470	49.99%
	G723		512	41.98%		512	43.28%
Configuration 4 Dual Xeon With Hyperthreading	μ-Law	DP	200	50.31%	LD	245	50.33%
	G726 32k		380	50.40%		310	50.36%
	G726 16k		495	50.15%		475	49.95%
	GSM		512	47.90%		512	44.34%
	G729a		512	45.10%		480	50.08%
	G723		512	34%		512	42.67%

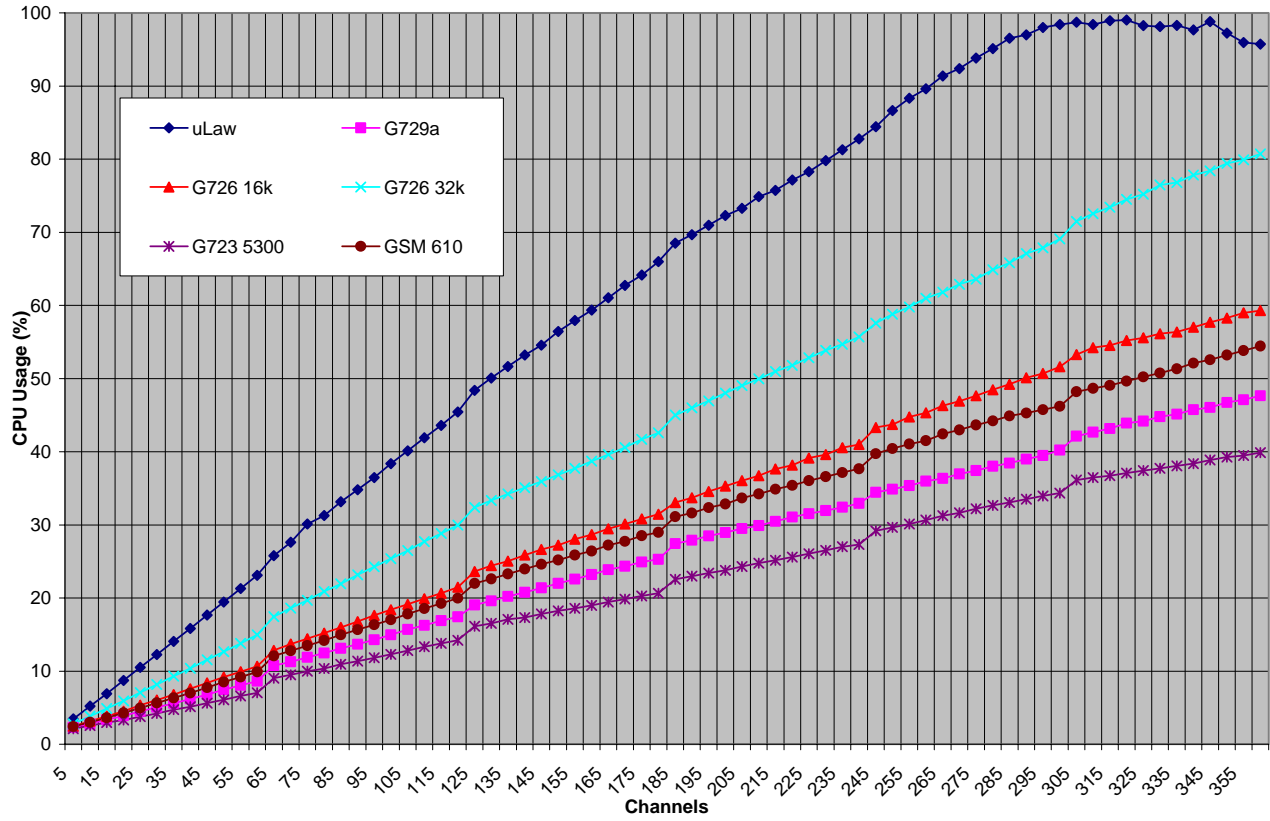
Table 1 - Channel capacity at 50% CPU loading

## Detailed Results

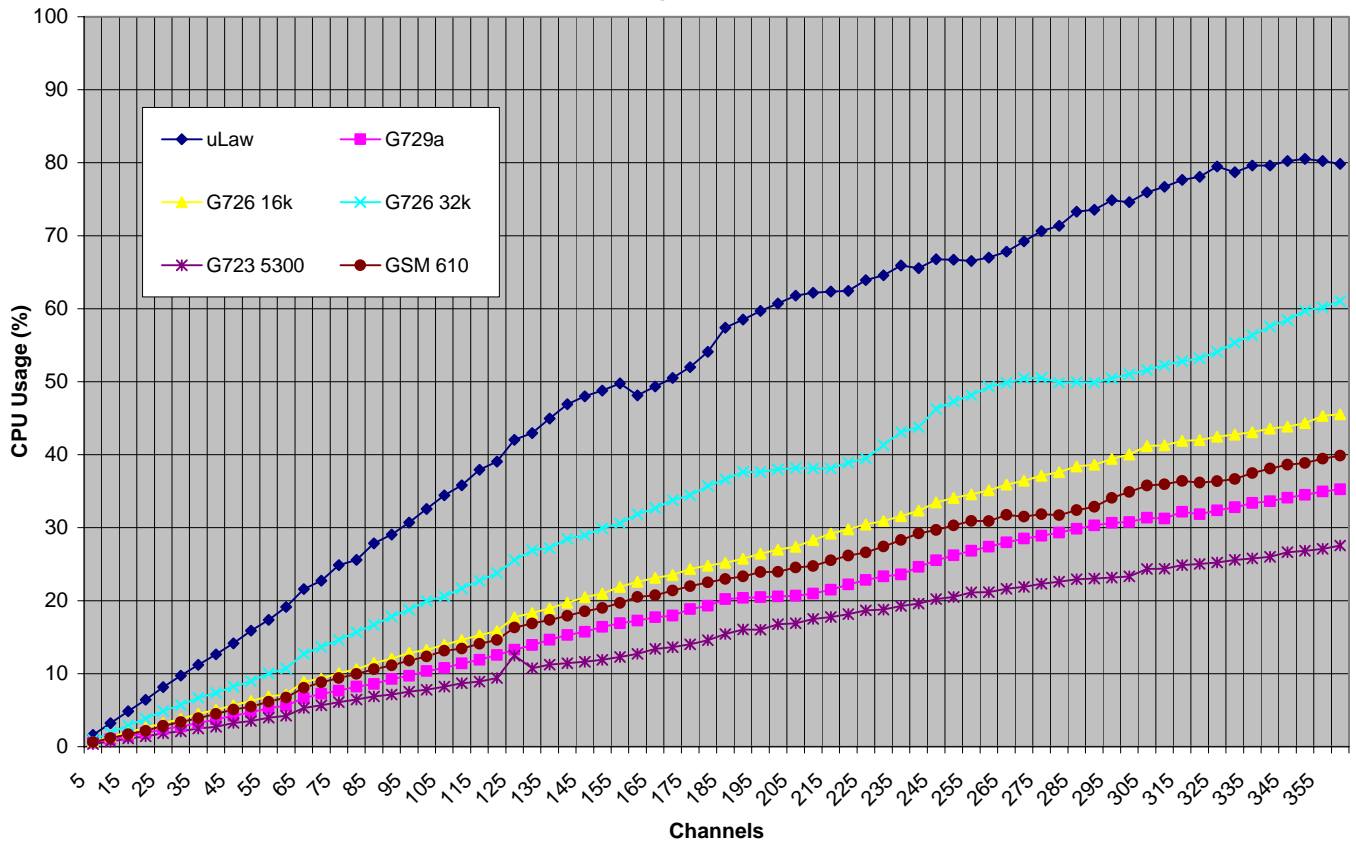
DP on System 1



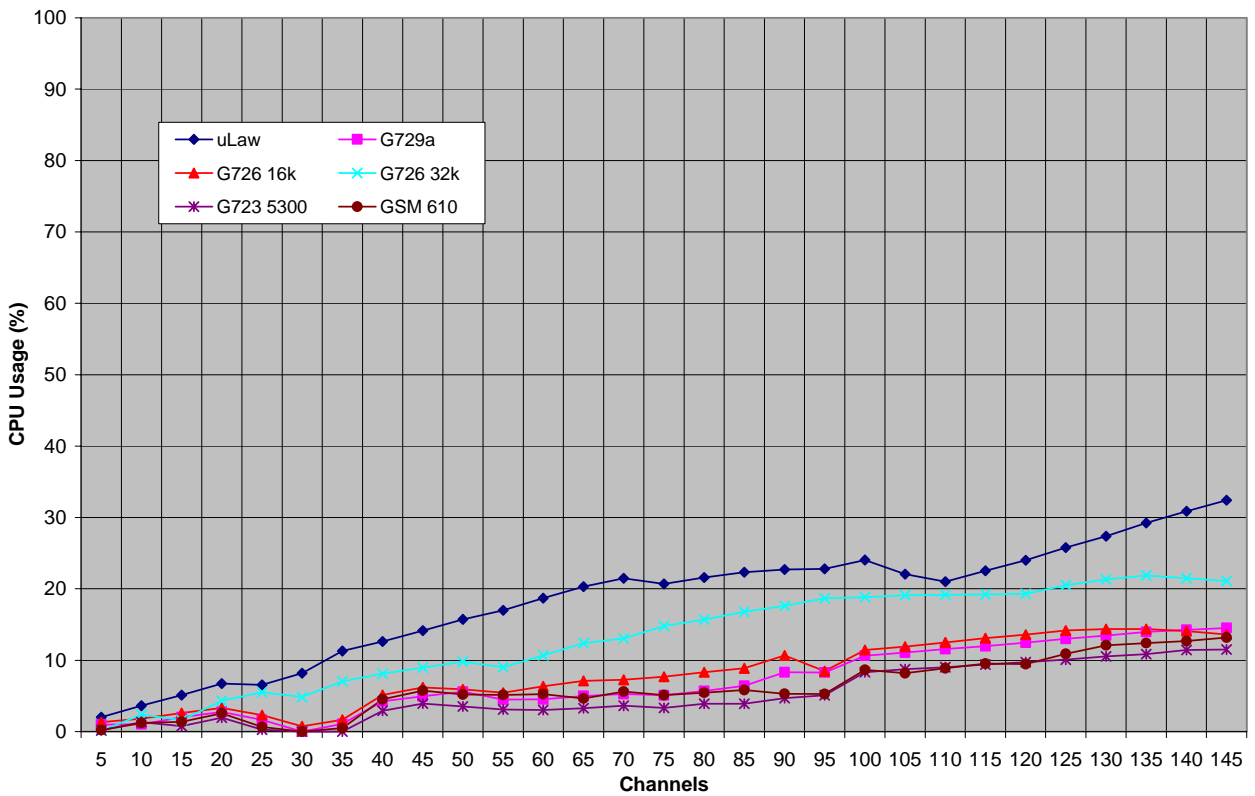
DP6409 Single Xeon w/o HT (System 3)

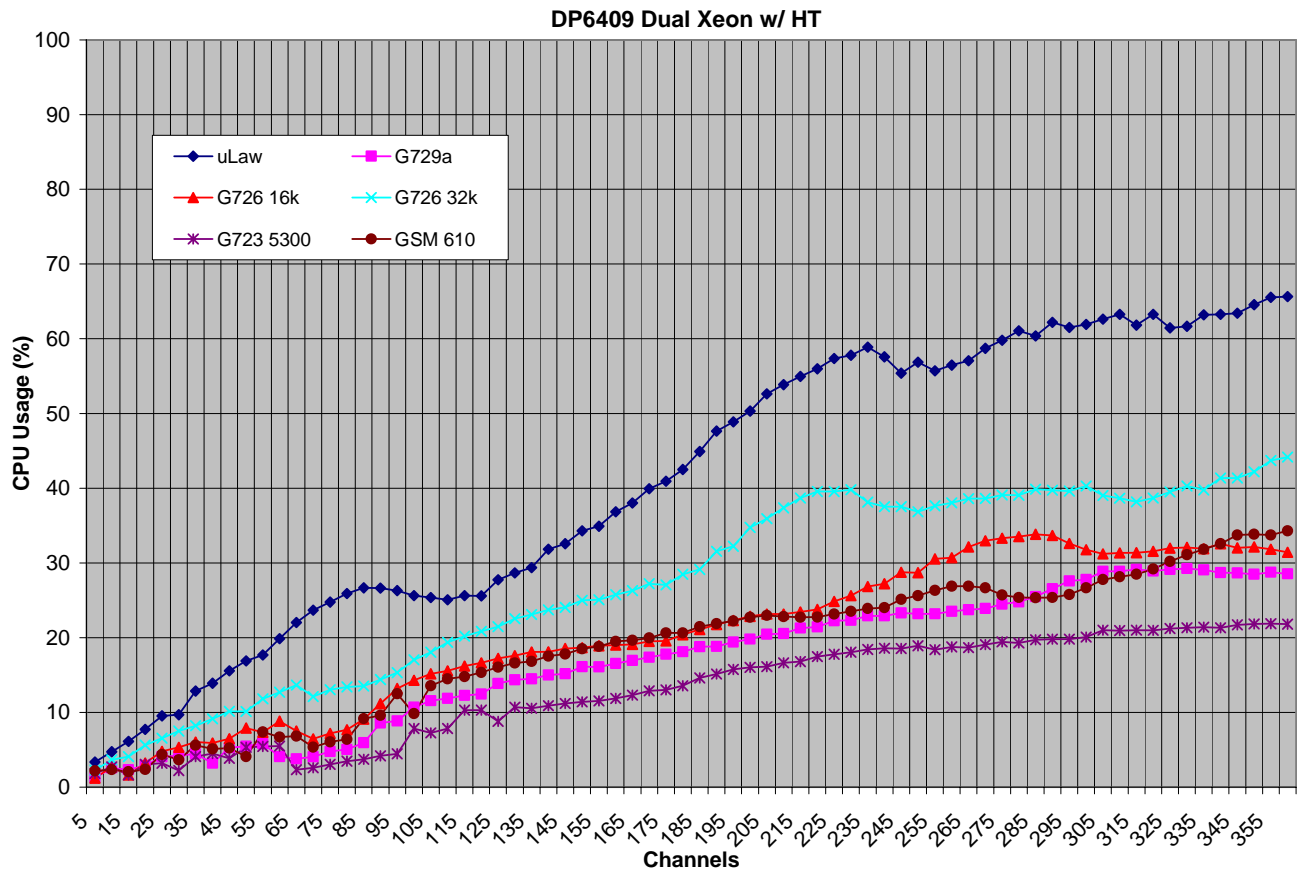
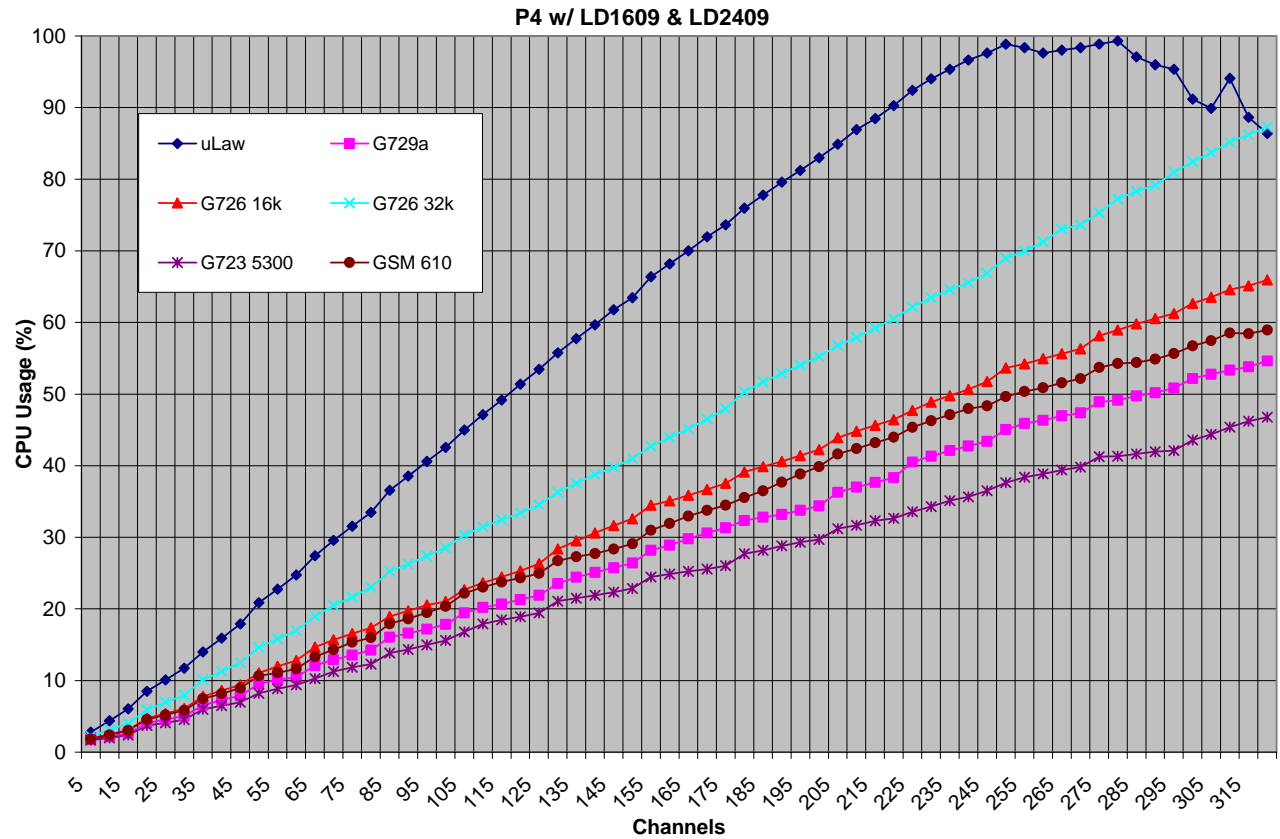


**DP6409 Single Xeon w/ HT**

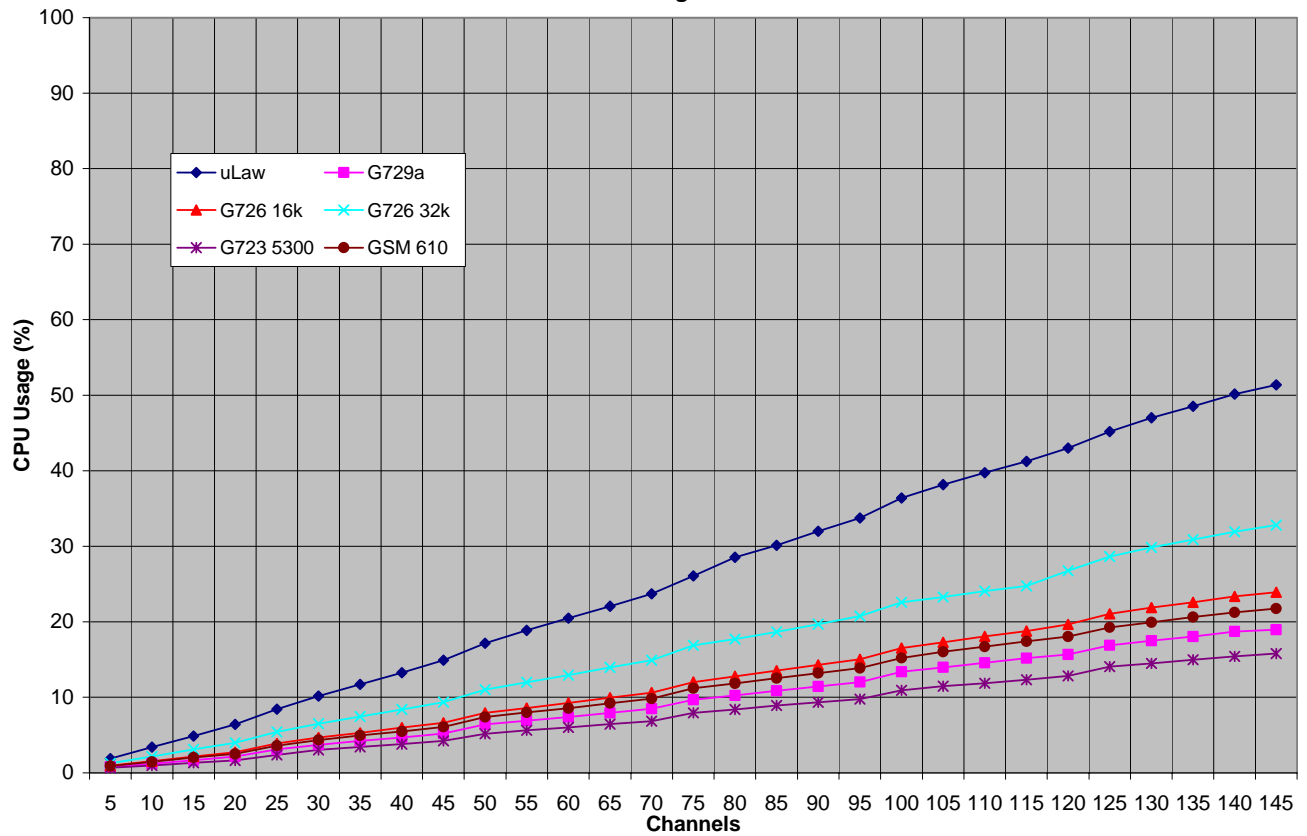


**LD2409 Dual Xeon w/ HT**



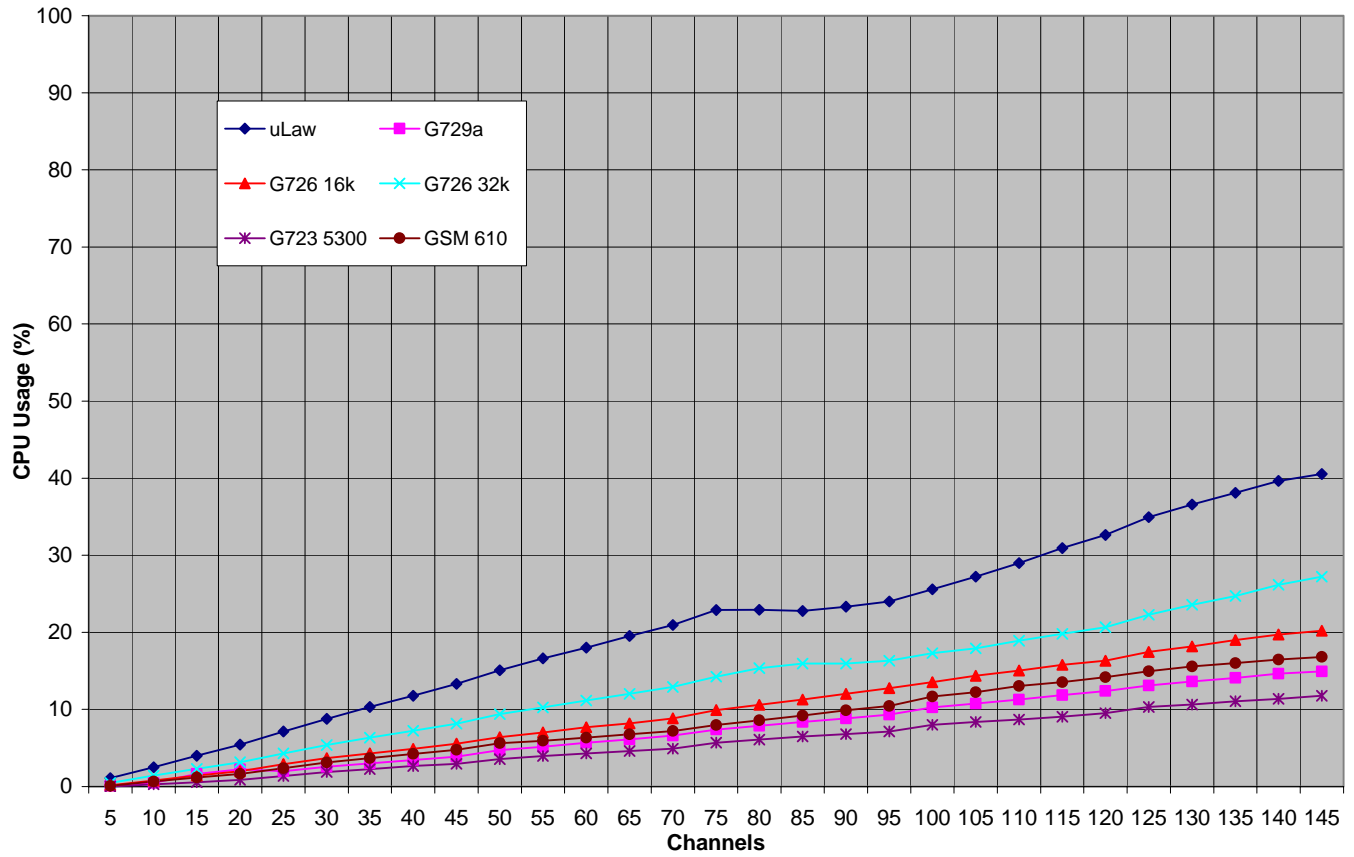


LD2409 Single Xeon w/o HT





LD2409 Single Xeon w/ HT



NGX on P4 (System 1)

